ECHO CANCELLATION USING A VARIABLE OFFSET COMPARATOR

The present application may be related to subject matter disclosed in one or more of the following applications that are assigned to the same assignee as that of the present application:

U. S. Patent Application Serial No. 09/967,804, "Equalization of a Transmission Line Signal Using a Variable Offset Comparator", filed September 28, 2001.

U. S. Patent Application Serial No. 09/968,349, "Multi-Level Receiver Circuit With Digital Output Using a Variable Offset Comparator", filed September 28, 2001.

U. S. Patent Application Serial No. 09/967,666, "Voltage Margin Testing of a Transmission Line Analog Signal Using a Variable Offset Comparator in a Data Receiver Circuit", filed September 28, 2001.

U. S. Patent Application Serial No. 09/895,625, "Variable Offset Amplifier Circuit", filed June 29, 2001.

U. S. Patent Application Serial No. 09/960,821, "A Method and Apparatus for Outbound Wave Subtraction Using a Variable Offset Amplifier", filed September 21, 2001.

10/037,751

U. S. Patent Application Serial No. _____, "A/D Conversion Using a Variable Offset Comparator", filed on the same date as the present application.

Background

[0001] This invention is in general related to data communications and more particularly to an echo cancellation technique that can be applied to a transmission line signal received by an input/output (i.e., I/O) circuit of an integrated circuit device.

[0002] I/O circuits act as the interface between different logic functional units of an electrical system. The functional units may be implemented in separate integrated circuit dies (i.e., IC chips) of the system. These chips may be in separate IC packages that have been soldered to a printed wiring board (i.e., PWB). The chips communicate with each other over one or more

[0035] To determine the coefficients of the echo cancellation filter, a calibration process may be performed by which the amplitudes of the various peaks that appear in the distortion produced by echo in the transmission line signal are given binary values. **Fig. 6** illustrates a flow diagram of an embodiment of a process for digitizing a received training pulse that is being periodically repeated. The process results in assigning binary values to consecutive samples of the distortion that has been caused by an echo of the training pulse that has been previously transmitted.

[0036] Referring briefly to **Fig. 5**, the periodic training pulses are part of the waveform 502. The electronic system should be designed so that the receiver is aware that a training pulse, rather than valid driver data, is being periodically detected by the near end receiver. The pulses should be sufficiently spaced apart in time to allow the transmission line to settle (e.g., to allow reflections of a pulse to die out before each subsequent pulse is transmitted).

[0037] Returning to **Fig. 6**, operation begins with an analog to digital (i.e. A/D) conversion on an initial sample point of a training pulse, where this sample point has a non-zero signal level (operation 504). This conversion may be performed by the near end receiver itself, using the VOC 214 as connected in **Fig. 2** according to a successive approximation A/D conversion process. See, e.g., U. S. Patent Application Serial No. 10/037,751, entitled "A/D Conversion Using a Variable Offset Comparator", filed on the same date as the present application and assigned to the same assignee as that of the present application. Alternatively, other A/D conversion procedures may be used, including those that are performed by a dedicated, off-chip integrated circuit test system rather than an on-chip A/D conversion technique in the receiver. The process continues with operation 508.

[0038] In operation 508, a shift is performed to an adjacent sample point of the training pulse. The spacing between adjacent sample points should be small enough so that the pulse is sufficiently digitized to yield useful signal levels in view of the pulse width and in view of the echo distortion. After shifting to the adjacent sample point, the A/D conversion is repeated for that new sample point (operation 512). Operations 508 and 512 are thus repeated